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10/602,280	06/23/2003	Rajesh Kota	NWISP045	4184

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EXAMINER	
HIGA, BRENDAN Y	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/602,280	KOTA ET AL.
	Examiner	Art Unit
	Brendan Y. Higa	2153

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 April 2007.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

The examiner would like to note that this application has been transferred to a new examiner.

This Office action is in response to Applicant's request for reconsideration filed on April 25, 2007.

Claims 1-30 remain pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 9-11, 14-25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US 2004/0117510), hereafter referred to as Arimilli, in view of Attanasio et al. (US 5371852), hereafter referred to as Attanasio, in further view of Allen et al. (US 4663706) hereafter referred to as Allen.

As per claim 1, Arimilli discloses an interconnection controller (see interconnect – Arimilli page 2 paragraph 23; where the interconnect are coupled to a number of processing units), comprising:

an intra-cluster interface configured for coupling with intra-cluster links to a plurality of local nodes, the local nodes including local processors (see cluster/interconnected – Arimilli page 5 paragraph 41; where clusters are interconnected/coupled and the local nodes are processors; also see Arimilli figure 4a);

an inter-cluster interface configured for coupling with an inter-cluster link to a non-local interconnection controller in a non-local cluster (see clusters and network – Arimilli page 5 paragraph 41-42; where clusters can be interconnected to other clusters/non local via network interface); encapsulation logic configured to receive intra-cluster packets from the local nodes via the intra-cluster links (see packet transmitted – Arimilli page 5 paragraph 43; where the packets are encapsulated using the private protocol to pass to other clusters) and to encapsulate the intra-cluster packets as inter-cluster packets for transmission on the inter-cluster link (see communication between clusters and private protocol – see Arimilli page 5 paragraph 42-43; where packets are transmitted to the processors in the cluster, as an inter-cluster packet); and a module comprising a remote transmission buffer (see network unit – Arimilli page 5 paragraph 43; note that the unit transmits/accepts packets from other clusters), the module configured to: receive inter-cluster packets from the encapsulation logic (see packet/receive – Arimilli page 5 paragraph 43; note that the network unit receives inter-cluster packets ; see Arimilli figure 4a); store inter-cluster packets in the remote transmission buffer (see

packet/receive - Arimilli page 5 paragraph 43; note that the network unit stores/receives inter-cluster packets ; see Arimilli figure 4a and paragraph 45); forward inter-cluster packets for transmission on the inter-cluster link (see packet transmitted – Arimilli page 5 paragraph 43; where the packets are encapsulated using the private protocol to pass to other clusters); generate a special packet for transmission on the inter-cluster link (see special data packet – Arimilli page 5 paragraph 41); and forward the special packet for transmission on the inter-cluster link without storing the special packet in the remote transmission buffer (see packet transmitted – Arimilli page 5 paragraph 43; where the packets, including the special packet are encapsulated using the private protocol to pass/transmit to other clusters).

Arimili does not expressly teach the intra-cluster links arranged in a point-to-point architecture in the local cluster.

Furthermore, Arimilli does not disclose expressly the remote transmission buffer determine when the remote transmission buffer is empty;

However, in the same art of cluster networking, Attanasio teaches an "encapsulated cluster" using a fiber optic point-to-point switch as the interconnect 110 for communication between nodes 105-109 within the encapsulated network (see col. 7, lines 24-28 and Fig. 2). Furthermore, Attanasio also teaches the encapsulated cluster communicating with other clusters over a communications link 120 (see col. 1, lines 60-65) using a gateway 109, wherein messages that are transferred over the

communication link 120 from the encapsulated network 200 are modified so that the source address of the messages is the gateway address rather than the individual source node, in this way computers (or clusters) external to the encapsulated cluster 200 perceive the message as coming from the gateway computer on the network rather than the sending node within the encapsulated cluster 200 (see Fig. 2, and col. 5, lines 47-55).

One of skill in the art would have been motivated to combine the teachings of Arimili and Attanasio for arranging the intra-cluster in a point-to-point architecture, in order to provide the cluster with 5 times more bandwidth then that of a token ring (see col. 7, lines 25-28).

Furthermore, Allen teaches the remote transmission buffer determine when the remote transmission buffer is empty (see buffer not full flag – Allen column 8 line 3-10; note that the cluster module controller determines if the buffer is empty/not full via a flag);
Arimilli and Allen are analogous art since they both have similar problem solving area, which is packet data transmission between inter-cluster link. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli with the teaching of Allen. The motivation is to enable the efficient communication between the processors, when there is an empty buffer, the controller can start/control the sending of packets to the particular processor.

As per claim 2, the combination of Arimilli, Attanasio, and Allen further teaches the interconnection controller of claim 1, wherein the special packet comprises a control character (see special packet and command – Arimilli paragraph 43; note that the special packet comprises a control/command character).

As per claim 3, the combination of Arimilli, Attanasio, and Allen further teaches a reception buffer, the module (see packet/receive – Arimilli page 5 paragraph 43; note that the network unit receives inter-cluster packets ; see Arimilli figure 4a) being further configured to: receive a special packet from the inter-cluster link (see special data packet – Arimilli page 5 paragraph 41); and drop the special packet without storing the special packet in the reception buffer (see packet – Arimilli page 5 paragraph 43; where the packets, including the special packet are encapsulated using the private protocol to pass/transmit to other clusters, but not stored in buffers).

As per claim 4, the combination of Arimilli, Attanasio, and Allen further teaches all the limitations of the parent claim 1 from which claim 4 depend (see above rejection for claim 1),

Arimilli does not disclose expressly wherein the module is configured to determine when the transmission buffer is empty by inspecting a single buffer space of the transmission buffer.

Allen discloses wherein the module is configured to determine when the transmission buffer is empty by inspecting a single buffer space of the transmission buffer (see buffer

not full flag – Allen column 8 line 3-10; note that the cluster module controller determines if the buffer is empty/not full via a flag, also see transmission – Allen column 8 line 11-14).

Arimilli and Allen are analogous art since they both have similar problem solving area, which is packet data transmission between inter-cluster link. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli with the teaching of Allen. The motivation is to enable the efficient communication between the processors, when there is an empty buffer, the controller can start/control the sending of packets to the particular processor.

As per claim 5, the combination of Arimilli, Attanasio, and Allen further teaches wherein the transmission buffer is an asynchronous buffer (see interconnect busses – Arimilli page 3 paragraph 32) that is configured to receive inter-cluster packets from the encapsulation logic at a first clock speed and forwards the inter-cluster packets at a second clock speed (see processing and passing – see Arimilli page 4 paragraph 36; note that the inter-cluster packets, or data within the cluster of processors are processed in a pipelined manner).

As per claim 9, the combination of Arimilli, Attanasio, and Allen further teaches an integrated circuit comprising the interconnection controller (see integrated circuit – Arimilli page 2 paragraph 23; note that the interconnect system comprises integrated circuits).

As per claim 10, the combination of Arimilli, Attanasio, and Allen further teaches a set of semiconductor processing masks representative of at least a portion of the interconnection controller (see integrated circuit – Arimilli page 2 paragraph 23; note that the interconnect system comprises integrated circuits which are processed using semiconductor masks).

As per claim 11, the combination of Arimilli, Attanasio, and Allen further teaches at least one computer-readable medium having data structures stored therein representative of the interconnection controller (see Arimilli page 1 paragraph 13; note the system is includes a computer readable medium such as registers).

As per claim 14, the combination of Arimilli, Attanasio, and Allen further teaches the integrated circuit comprises an application-specific integrated circuit (see integrated circuit – Arimilli page 2 paragraph 23; note that the circuit is intended for a specific application).

As per claim 15, the combination of Arimilli, Attanasio, and Allen further teaches the data structures comprise a simulatable representation of the interconnection controller (see Arimilli page 1 paragraph 13; note the system is includes a data structures in registers which are simulatable).

As per claim 16, the combination of Arimilli, Attanasio, and Allen further teaches the data structures comprise a code description of the interconnection controller (see Arimilli page 1 paragraph 13; note the system is includes a data structures in registers).

As per claim 17, the combination of Arimilli, Attanasio, and Allen further teaches the simulatable representation comprises a netlist (see integrated circuit – Arimilli page 2 paragraph 23; note that the interconnect system comprises integrated circuits which are represented during simulations as a netlist).

As per claim 18, the combination of Arimilli, Attanasio, and Allen further teaches the code description corresponds to a hardware description language (see integrated circuit – Arimilli page 2 paragraph 23; note that the interconnect system comprises integrated circuits which are designed/coded using hardware description language)

As per claim 19, Arimilli discloses a computer system, comprising: a first cluster including a first plurality of processors and a first interconnection controller, the first interconnection controller comprising (see interconnect – Arimilli page 2 paragraph 23; where the interconnect is coupled to a number of processing units): encapsulation logic configured to receive intra-cluster packets from the first plurality of processors via the first point-to-point intra-cluster links (see cluster/interconnected – Arimilli page 5 paragraph 41; where clusters are interconnected/coupled and the local nodes are processors; also see Arimilli figure 4a) and to encapsulate the intra-cluster packets as

high-speed link packets for transmission on an inter-cluster link (see communication between clusters and private protocol – see Arimilli page 5 paragraph 42-43; where packets are transmitted to the processors in the cluster, as an inter-cluster packet); and a first module comprising a transmission buffer (see network unit – Arimilli page 5 paragraph 43; note that the unit transmits/accepts packets from other clusters), the first module configured to: receive high-speed link packets from the encapsulation logic (see packet/receive – Arimilli page 5 paragraph 43; note that the network unit receives inter-cluster packets ; see Arimilli figure 4a); store high-speed link packets in a transmission buffer (see packet/receive - Arimilli page 5 paragraph 43; note that the network unit stores/receives inter-cluster packets ; see Arimilli figure 4a and paragraph 45); forward high-speed link packets for transmission on the inter-cluster link (see packet transmitted – Arimilli page 5 paragraph 43; where the packets are encapsulated using the private protocol to pass to other clusters); generate a special packet responsive to the empty condition (see special data packet – Arimilli page 5 paragraph 41); and forward the special packet to the inter-cluster link without storing the special packet in the transmission buffer (see packet transmitted – Arimilli page 5 paragraph 43; where the packets, including the special packet are encapsulated using the private protocol to pass/transmit to other clusters).

Arimili does not expressly teach the first plurality of processors and the first interconnection controller interconnected by first point-to-point intra-cluster links.

Furthermore, Arimilli does not disclose expressly determining an empty condition indicating that the transmission buffer is empty;

However, in the same art of cluster networking, Attanasio teaches an “encapsulated cluster” using a fiber optic point-to-point switch as the interconnect 110 for communication between nodes 105-109 within the encapsulated network (see col. 7, lines 24-28 and Fig. 2). Furthermore, Attanasio also teaches the encapsulated cluster communicating with other clusters over a communications link 120 (see col. 1, lines 60-65) using a gateway 109, wherein messages that are transferred over the communication link 120 from the encapsulated network 200 are modified so that the source address of the messages is the gateway address rather than the individual source node, in this way computers (or clusters) external to the encapsulated cluster 200 perceive the message as coming from the gateway computer on the network rather than the sending node within the encapsulated cluster 200 (see Fig. 2, and col. 5, lines 47-55).

One of skill in the art would have been motivated to combine the teachings of Arimili and Attanasio for arranging the intra-cluster in a point-to-point architecture, in order to provide the cluster with 5 times more bandwidth then that of a token ring (see col. 7, lines 25-28).

Allen teaches determining an empty condition indicating that the transmission buffer is empty (see buffer not full flag – Allen column 8 line 3-10; note that the cluster module controller determines if the buffer is empty/not full via a flag);

Arimilli and Allen are analogous art since they both have similar problem solving area, which is packet data transmission between inter-cluster link. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli with the teaching of Allen. The motivation is to enable the efficient communication between the processors, when there is an empty buffer, the controller can start/control the sending of packets to the particular processor.

As per claim 20, the combination of Arimilli, Attanasio, and Allen further teaches all the limitations of the parent claim 19 from which claim 20 depend (see above rejection for claim 19).

Arimilli discloses a second cluster (note that there are a plurality of interconnects/clusters see Arimilli Figure 4a) including a second plurality of processors and a second interconnection controller, the second plurality of processors and the second interconnection controller interconnected by second point-to-point intra-cluster links, the second interconnection controller comprising a second module configured to (see interconnect – Arimilli page 2 paragraph 23; where the interconnect are coupled to a number of processing units/clusters): receive high-speed link packets from the inter-cluster link (see packet/receive – Arimilli page 5 paragraph 43; note that the network unit receives inter-cluster packets ; see Arimilli figure 4a); store the high-speed link

packets in a reception buffer (see packet/receive - Arimilli page 5 paragraph 43; note that the network unit receives/stores inter-cluster packets ; see Arimilli figure 4a and paragraph 45), receive the special packet (see special data packet – Arimilli page 5 paragraph 41); and drop the special packet without storing the special packet in the reception buffer (see packet – Arimilli page 5 paragraph 43; where the packets, including the special packet are encapsulated using the private protocol to pass/transmit to other clusters).

As per claim 21, the combination of Arimilli, Attanasio, and Allen further teaches wherein the special packet comprises a control character (see special packet and command – Arimilli paragraph 43; note that the special packet comprises a control/command character).

As per claim 22, the combination of Arimilli, Attanasio, and Allen teaches the invention substantially as claimed as noted above. Furthermore, Arimilli teaches a computer system comprising a plurality of processor clusters interconnected by a plurality of point-to-point inter-cluster links, each processor cluster comprising nodes including a plurality of local processors and an interconnection controller (see interconnect – Arimilli page 2 paragraph 23; where the interconnect are coupled to a number of processing units), communications within a cluster being made via an intra-cluster protocol that uses intra-cluster packets (see communication between clusters and private protocol – see Arimilli page 5 paragraph 42-43; where packets are transmitted to the processors in the

cluster), wherein the interconnection controller in each cluster is operable to map locally-generated communications directed to others of the clusters to the point-to-point inter-cluster links (see addresses – Arimilli page 5 paragraph 41; note that the communications are mapped using the addresses) and to map remotely-generated communications directed to the local nodes to the point-to-point intra-cluster links (see network unit – Arimilli page 5 paragraph 43; note that the unit transmits/accepts packets from other clusters), communications between clusters being made via an inter-cluster protocol that uses inter-cluster packets (see communication between clusters and private protocol – see Arimilli page 5 paragraph 42-43), an inter-cluster packet encapsulating at least one intra-cluster packet, each interconnection controller configured to generate (see cluster/interconnected – Arimilli page 5 paragraph 41; where clusters are interconnected/coupled and the local nodes are processors; also see Arimilli figure 4a) and transmit a special packet on an inter-cluster link when the interconnection controller has no valid inter-cluster packets to send (see special data packet – Arimilli page 5 paragraph 41), the special packet not being stored in a transmission buffer prior to being transmitted on the inter-cluster link (see packet – Arimilli page 5 paragraph 43; where the packets, including the special packet are encapsulated using the private protocol to pass/transmit to other clusters).

Arimilli does not expressly teach the interconnection controller, interconnected by a plurality of point-to-point intra-cluster links.

However, in the same art of cluster networking, Attanasio teaches an "encapsulated cluster" using a fiber optic point-to-point switch as the interconnect 110 for communication between nodes 105-109 within the encapsulated network (see col. 7, lines 24-28 and Fig. 2). Furthermore, Attanasio also teaches the encapsulated cluster communicating with other clusters over a communications link 120 (see col. 1, lines 60-65) using a gateway 109, wherein messages that are transferred over the communication link 120 from the encapsulated network 200 are modified so that the source address of the messages is the gateway address rather than the individual source node, in this way computers (or clusters) external to the encapsulated cluster 200 perceive the message as coming from the gateway computer on the network rather than the sending node within the encapsulated cluster 200 (see Fig. 2, and col. 5, lines 47-55).

One of skill in the art would have been motivated to combine the teachings of Arimili and Attanasio for arranging the intra-cluster in a point-to-point architecture, in order to provide the cluster with 5 times more bandwidth then that of a token ring (see col. 7, lines 25-28).

As per claim 23, the combination of Arimilli, Attanasio, and Allen further teaches wherein the special packet comprises a control character (see special packet and command – Arimilli paragraph 43; note that the special packet comprises a control/command character).

As per claim 24, the combination of Arimilli, Attanasio, and Allen further teaches each interconnection controller being further configured to receive a special packet (see packet/receive – Arimilli page 5 paragraph 43; note that the network unit receives inter-cluster packets, including special packets; see Arimilli page 5 paragraph 41), but not to store the special packet in a reception buffer for storing valid inter-cluster packets (see packet – Arimilli page 5 paragraph 43; where the packets, including the special packet are encapsulated using the private protocol to pass/transmit to other clusters, but not stored in buffers).

As per claim 25, the combination of Arimilli, Attanasio, and Allen further teaches the transmission buffer is an asynchronous buffer that receives inter-cluster packets (see interconnect busses – Arimilli page 3 paragraph 32) at a first clock speed and forwards the inter-cluster packets at a second clock speed for transmission on the inter-cluster link (see processing and passing – see Arimilli page 4 paragraph 36; note that the inter-cluster packets, or data within the cluster of processors are processed in a pipelined manner).

As per claim 28, Arimilli discloses a computer-implemented method for decreasing latency in a computer system comprising a plurality of clusters, each cluster including a plurality of local nodes and an interconnection controller (see interconnect – Arimilli page 2 paragraph 23; where the interconnect are coupled to a number of processing units), communications between the local nodes and the interconnection controller

made via an intra-cluster protocol using intra-cluster, the interconnection controller of each cluster interconnected by inter-cluster links with the interconnection controller of other clusters (see communication between clusters and private protocol – see Arimilli page 5 paragraph 42-43; where packets are transmitted to the processors in the cluster, as an inter-cluster packet), the computer-implemented method comprising: forming inter-cluster packets by encapsulating intra-cluster packets (see packet transmitted – Arimilli page 5 paragraph 43; where the packets are encapsulated using the private protocol to pass to other clusters); storing the inter-cluster packets in a remote transmission buffer of a first interconnection controller; transmitting the inter-cluster packets to a second interconnection controller (see packet/receive - Arimilli page 5 paragraph 43; note that the network unit stores/receives inter-cluster packets and also pass/transmit packets to other clusters ; see Arimilli figure 4a and paragraph 45); storing received inter-cluster packets in a reception buffer of the second interconnection controller (see packet/receive - Arimilli page 5 paragraph 43; note that the network unit stores/receives inter-cluster packets ; see Arimilli figure 4a and paragraph 45); generating a control character in response to a determination that the remote transmission buffer is empty (see special data packet – Arimilli page 5 paragraph 41; also see special packet and command, Arimilli paragraph 43; note that the special packet comprises a control/command character); transmitting the control character to the second interconnection controller (see packet – Arimilli page 5 paragraph 43; where the packets, including the special packet comprising a control character are encapsulated using the private protocol to pass/transmit to other clusters); and dropping

the control character without storing the control character in the reception buffer (see packet – Arimilli page 5 paragraph 43; where the packets, including the special packet are encapsulated using the private protocol to pass/transmit to other clusters, but not stored in buffers).

Arimilli does not expressly teach the interconnection controller interconnected by point-to-point intra-cluster links. Furthermore, Arimilli does not disclose expressly determining that the remote transmission buffer is empty.

However, in the same art of cluster networking, Attanasio teaches an "encapsulated cluster" using a fiber optic point-to-point switch as the interconnect 110 for communication between nodes 105-109 within the encapsulated network (see col. 7, lines 24-28 and Fig. 2). Furthermore, Attanasio also teaches the encapsulated cluster communicating with other clusters over a communications link 120 (see col. 1, lines 60-65) using a gateway 109, wherein messages that are transferred over the communication link 120 from the encapsulated network 200 are modified so that the source address of the messages is the gateway address rather than the individual source node, in this way computers (or clusters) external to the encapsulated cluster 200 perceive the message as coming from the gateway computer on the network rather than the sending node within the encapsulated cluster 200 (see Fig. 2, and col. 5, lines 47-55).

One of skill in the art would have been motivated to combine the teachings of Arimili and Attanasio for arranging the intra-cluster in a point-to-point architecture, in order to provide the cluster with 5 times more bandwidth then that of a token ring (see col. 7, lines 25-28).

Furthermore, Allen teaches determining that the remote transmission buffer is empty (see buffer not full flag – Allen column 8 line 3-10; note that the cluster module controller determines if the buffer is empty/not full via a flag).

Arimilli and Allen are analogous art since they both have similar problem solving area, which is packet data transmission between inter-cluster link. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli with the teaching of Allen. The motivation is to enable the efficient communication between the processors, when there is an empty buffer, the controller can start/control the sending of packets to the particular processor.

Claims 7, 26-27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (US 2004/0117510), in view of Attanasio (US 5371852), in further view of Allen (US 4663706) and further in view of Keller (US 6938094).

As per claim 7, the combination of Arimilli, Attanasio, and Allen teaches all the limitations of the parent claim 1 from which claim 7 depend (see above rejection for claim 1).

Furthermore, the combination of Arimilli, Attanasio, and Allen discloses a local transmitter configured to: receive intra-cluster packets from the from the local nodes via the intra-cluster links (see packet – Arimilli page 5 paragraph 43; where the packets are encapsulated using the private protocol to pass to other clusters); store intra-cluster packets in a local transmission buffer (see packet/receive - Arimilli page 5 paragraph 43; note that the network unit receives/stores inter-cluster packets ; see Arimilli figure 4a and paragraph 45); forward intra-cluster packets for transmission on the intra-cluster links (see packet transmitted – Arimilli page 5 paragraph 43; where the packets are encapsulated using the private protocol to pass to other clusters);

The combination of Arimilli, Attanasio, and Allen Arimilli-Allen does not disclose expressly determining when there are no valid intra-cluster packets to transmit; generate NOP packets when there are no valid intra-cluster packets to transmit; forward the NOP packets to the local transmission buffer; and transmit the NOP packets on the intra-cluster links.

Keller teaches determining when there are no valid intra-cluster packets to transmit (see buffer free indication – Keller column 9 line 61-65; note that the indication is a determination that no packets are present, ie: the buffer is free); generate NOP packets when there are no valid intra-cluster packets to transmit (no operation packet – Keller column 9 lines 61-65); forward the NOP packets to the local transmission buffer; and transmit the NOP packets on the intra-cluster links (see column 10 lines 4-19; note that the packets, including the NOP packet, are on the intra cluster link/channel).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli, Attanasio and Allen with the teaching of Keller. The motivation is to enable the efficient communication between the processors, when no packets are transmitted, the controller can start/control the sending of packets to the particular processor.

As per claim 26, the combination of Arimilli, Attanasio, and Allen discloses all the limitations of the parent claim 22 from which claim 26 depend (see above rejection for claim 22),

the combination of Arimilli, Attanasio, and Allen not disclose expressly each interconnection controller is further configured to generate a NOP packet when the interconnection controller has no valid intra-cluster packets to send.

Keller teaches each interconnection controller is further configured to generate a NOP packet (no operation packet – Keller column 9 lines 61-65) when the interconnection controller has no valid intra-cluster packets to send (see buffer free indication – Keller column 9 line 61-65; note that the indication is a determination that no packets are present, ie: the buffer is free).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli-Allen with the teaching of Keller. The motivation is to enable the efficient communication between the processors, when no packets are transmitted, the controller can start/control the sending of packets to the particular processor.

As per claim 27, the combination of Arimilli, Attanasio, and Allen teachesall the limitations of the parent claim 26 from which claim 27 depend (see above rejection for claim 26),

The combination of Arimilli, Attanasio, and Allen does not disclose each interconnection controller is further configured to forward the NOP packet to a local transmission buffer to await transmission on an intra-cluster link.

Keller teaches each interconnection controller is further configured to forward the NOP packet to a local transmission buffer to await transmission on an intra-cluster link (see column 10 lines 4-19; note that the packets, including the NOP packet, are on the intra cluster link/channel).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli-Attanasio-Allen with the teaching of Keller. The motivation is to enable the efficient communication between the processors, when no packets are transmitted, the controller can start/control the sending of packets to the particular processor.

As per claim 30, the combination of Arimilli, Attanasio, and Allen teaches all the limitations of the parent claim 28 from which claim 30 depend (see above rejection for claim 28).

The combination of Arimilli, Attanasio, and Allen does not disclose expressly determining that there are no valid intra-cluster packets for transmission on the point-to-

point intra-cluster links; generating NOP packets; storing the NOP packets in a local transmission buffer; and transmitting the NOP packets to local nodes on the point-to-point intra-cluster links.

Keller teaches determining that there are no valid intra-cluster packets for transmission on the point-to-point intra-cluster links (see buffer free indication – Keller column 9 line 61-65; note that the indication is a determination that no packets are present, ie: the buffer is free); generating NOP packets (no operation packet – Keller column 9 lines 61-65); storing the NOP packets in a local transmission buffer (see buffer – Keller column 10 lines 56-65; note that packets are stored in the buffers, including the NOP packet); and transmitting the NOP packets to local nodes on the point-to-point intra-cluster links (see column 10 lines 4-19; note that the packets, including the NOP packet, are on the intra cluster link/channel).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli, Attanasio, and Allen with the teaching of Keller. The motivation is to enable the efficient communication between the processors, when no packets are transmitted, the controller can start/control the sending of packets to the particular processor.

Claims 6, 8, 12, 13, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (US 2004/0117510), in view of Attanasio (US 5371852), in further view of Allen (US 4663706) and further in view of Henson (US 6158014).

As per claim 6, the combination of Arimilli, Attanasio, and Allen teaches all the limitations of the parent claim 1 from which claim 6 depend (see above rejection for claim 1).

The combination of Arimilli, Attanasio, and Allen does not disclose expressly wherein the module is configured to initialize the inter-cluster link and use information obtained during an initialization process to perform de-skewing operations on packets received on the inter-cluster link.

Henson teaches wherein the module is configured to initialize the inter-cluster link and use information obtained during an initialization process to perform de-skewing operations on packets received on the inter-cluster link (see pattern recognition – Henson column 4 lines 33-40; also see Henson column 4 lines 41-46).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli, Attanasio, and Allen with the teaching of Henson. The motivation would be to enable the synchronizing of incoming data since the received data might be transmitted with a different clock speeds; also to enable the decoding of incoming data since the received data might be transmitted are encoded differently.

As per claim 8, the combination of Arimilli, Attanasio, and Allen teaches discloses a serializer for serializing inter-cluster packets (see sectors – Arimilli page 5 paragraph 43; note that the packets are striped into sectors).

The combination of Arimilli, Attanasio, and Allen teaches does not disclose expressly performing bit conversion of inter-cluster packets.

Henson teaches performing bit conversion of inter-cluster packets (see Henson column 4 lines 1-5; note that the bitstream data is used by the deserializer, which generate multiple bit characters/bit conversion).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli-Attanasio-Allen with the teaching of Henson. The motivation would be to enable the decoding of incoming data since the received data might be transmitted are encoded differently.

As per claim 12, Arimilli-Attanasio-Allen-Henson discloses all the limitations of the parent claim 8 from which claim 12 depend (see above rejection for claim 8).

The combination of Arimilli, Attanasio, and Allen teaches does not disclose expressly wherein the bit conversion encodes clock data in the inter-cluster packets.

Henson teaches wherein the bit conversion encodes clock data in the inter-cluster packets (see clock speed – Henson column 2 lines 33-45; note that the data received include clock speed data; also see column 2 lines 61-64).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli-Attanasio-Allen with the teaching of Henson. The motivation would be to enable the synchronizing of incoming data since the received data might be transmitted with a different clock speeds.

As per claim 13, Arimilli-Attanasio-Allen-Henson discloses all the limitations of the parent claim 8 from which claim 13 depend (see above rejection for claim 8).
Furthermore, Henson teaches wherein the bit conversion comprises 8b/10b conversion (see 8b/10b – Henson column 1 lines 49-54; note that Henson teaches 8b/10 conversion used for interconnection networks; also see Henson claim 11).
At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli-Attanasio-Allen with the teaching of Henson. The motivation would be to enable the incoming data for use in high-speed networks that use Gigabit Ethernet or fibre channels, since these technologies transmit data using the 8b/10b encoding.

As per claim 29, Arimilli-Allen discloses all the limitations of the parent claim 28 from which claim 29 depend (see above rejection for claim 28).
The combination of Arimilli, Attanasio, and Allen teaches does not disclose expressly performing an initialization sequence that establishes a characteristic skew pattern between data lanes of the inter-cluster link; encoding clock data in each symbol transmitted on the inter-cluster link; recovering clock data from each symbol received on the inter-cluster link; and applying the characteristic skew pattern to correct for skew between data lanes of the inter-cluster link.
Henson teaches performing an initialization sequence that establishes a characteristic skew pattern between data lanes of the inter-cluster link (see pattern recognition – Henson column 4 lines 33-40); encoding clock data in each symbol transmitted on the

inter-cluster link (see clock speed – Henson column 2 lines 33-45; note that the data received include clock speed data; also see column 2 lines 61-64); recovering clock data from each symbol received on the inter-cluster link (see clock control signal – Henson column 4 lines 28-32); and applying the characteristic skew pattern to correct for skew between data lanes of the inter-cluster link (see pattern recognition – Henson column 4 lines 41-46; note that the system applies the pattern to the bitstream/data lanes).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Arimilli-Attanasio-Allen with the teaching of Henson. The motivation would be to enable the synchronizing of incoming data since the received data might be transmitted with a different clock speeds; also to enable the decoding of incoming data since the received data might be transmitted are encoded differently.

Response to Arguments

Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brendan Y. Higa whose telephone number is (571)272-5823. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (571)272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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